WHAT IS CLAIMED IS:

1. A semiconductor chip assembly of the type including a semiconductor chip having a plurality of surfaces and having contacts on at least one of said surfaces and a flexible sheetlike element having terminals thereon electrically connected to said contacts, characterized in that said sheetlike element and at least some of said terminals overlie one said surface of said chip, said terminals are movable with respect to said chip and the assembly includes resilient means for permitting movement of said terminals toward said chip.

2. An assembly as claimed in claim 1 further characterized in that said resilient means include a compliant layer disposed between said terminals and said chip so that said compliant layer will be compressed upon movement of said terminals toward said chip.

3. A chip assembly as claimed in claim 2 further characterized in that said compliant layer is formed from an elastomeric material.

4. A chip assembly as claimed in claim 2 further characterized in that said compliant layer includes masses of a low modulus material and holes interspersed with said masses of low modulus material, said masses of said low modulus material being aligned with said terminals, said holes in said compliant layer being out of alignment with said terminals.

5. A chip assembly as claimed in claim 1 or claim 2 or Claim 3 or claim 4 further characterized in that said chip has a front surface, said contacts are disposed on said front surface and said sheetlike element and said terminals overlie said front surface of said chip.

6. A chip assembly as claimed in claim 1 or claim 2 or claim 3 or claim 4 further characterized in that said chip has oppositely-facing front and rear surfaces, said contacts are disposed on said front

surface, and said sheetlike element and said terminals overlie said rear surface of said chip.

7. A method of making a semiconductor chip assembly including the step of assembling a flexible, sheetlike element having terminals thereon to a semiconductor chip and connecting terminals on said sheetlike element to contacts on said chip, characterized in that said assembling step is conducted so that said terminals on said sheetlike element overlie a surface of the chip and in that the assembly includes resilient means for permitting movement of said terminals towards said surface of said chip.

8. A method as claimed in claim 7 further characterized in that a compliant layer is disposed between said chip and said terminals to provide said resilient means.

9. A method as claimed in claim 7 further characterized by the step of testing the chip by establishing temporary electrical contact between a plurality of test probes and said terminals whereby said resilient means will permit displacement of at least some of said central terminals toward said chip surface during said step of establishing temporary electrical contact.

10. A method as claimed in claim 9 further characterized in that said step of establishing temporary electrical contact includes the step of simultaneously establishing temporary contact between a plurality of said terminals and a plurality of test probes rigidly connected to a test fixture.

11. A method as claimed in claim 7 further characterized in that said step of connecting said terminals on said sheetlike element includes the step of connecting flexible leads so that such leads extend between the contacts and terminals through at least one aperture in said sheetlike element.

12. A method as claimed in claim 11 further characterized in that said sheetlike element has said

terminals and prefabricated leads positioned thereon prior to said assembling step.

13. A method as claimed in claim 12 further characterized in that said step of connecting said leads includes the step of bonding said prefabricated leads to said contacts on said chip in said at least one aperture by inserting a tool into each said aperture.

14. A method as claimed in claim 7 further characterized by the steps of assembling a substrate with said interposer so that contact pads on a substrate confront the terminals on said sheetlike element and bonding said terminals to said pads.

15. A component for assembly to a semiconductor chip including a flexible sheetlike element having terminals thereon, characterized by a compliant layer underlying said terminals.

16. A component as claimed in claim 15 further characterized in that said compliant layer includes masses of a low modulus material and holes interspersed with said masses of low modulus material, said masses of said low modulus material being aligned with said terminals, said holes in said compliant layer being out of alignment with said terminals.

17. A component as claimed in claim 16 further characterized in that said sheetlike element includes a thin, flexible top layer formed from a material selected from the group consisting of thermoset and thermoplastic polymers overlying said compliant layer.

18. A component as claimed in claim 17 wherein said terminals are disposed on said top layer.

19. A component as claimed in claim 17 wherein said terminals are disposed between said top layer and said compliant layer, said top layer having apertures aligned with said terminals so that said terminals are accessible from a surface of said sheetlike element opposite from said compliant layer.

20. A component for use in semiconductor chip assemblies, the component including a sheetlike interposer having outboard edges, a plurality of terminals disposed on said interposer and a plurality of prefabricated leads connected to said terminals and having contact portions, said prefabricated leads being flexible, the contact portion of each said prefabricated lead being movable with respect to the terminal connected to such lead, characterized by at least one securement element integral with said interposer, each said securement element having an inboard edge extending generally parallel to one of said outboard edges of said interposer so that such parallel edges define an elongated slot, each such prefabricated lead extending to the vicinity of one said slot.

21. A component as claimed in claim 20 wherein the contact portion of each said prefabricated lead extends across said slot.

22. A semiconductor chip assembly of the type including:

(a) a semiconductor chip having a front surface defining the top of the chip, said front surface including a central region and a peripheral region surrounding said central region whereby said central region is disposed inwardly of said peripheral region, said chip having a plurality of peripheral contacts disposed in said peripheral region of said front surface, characterized by;

(b) a flexible, sheetlike dielectric interposer overlying said central region of said chip front surface, said interposer having a first surface facing toward said chip and a second surface facing away from said chip, said interposer having outboard edges disposed inwardly of said peripheral contacts;

(c) a plurality of central terminals disposed on said interposer and overlying said central region of said chip front surface; and

(d) a plurality of peripheral contact leads connecting at least some of said peripheral contacts and at least some of said central terminals, each said peripheral contact lead having a central terminal end overlying said interposer and connected to one of said central terminals and a contact end projecting outwardly beyond one of said edges of said interposer and connected to one of said peripheral contacts, whereby each said peripheral contact lead extends inwardly from one of said peripheral contacts to one of said central terminals on said interposer, said central terminals being movable with respect to said contacts.

23. A chip assembly as claimed in claim 22 further characterized in that at least some of said peripheral contact leads have outward extensions projecting outwardly beyond said peripheral contacts, and the assembly further includes at least one securement element disposed outwardly of said peripheral contacts and physically connected to a plurality of said outward extensions.

24. A chip assembly as claimed in claim 23 further characterized in that each said securement element has an inboard edge extending generally parallel to one of said outboard edges of said interposer so that such parallel edges define an elongated slot between each said securement element and said interposer, each said peripheral contact leads extending across one said slot.

25. A chip assembly as claimed in claim 24 further characterized by bridge elements extending between each said securement element and said interposer, said bridge elements being spaced apart from one another, said slots extending between said bridge elements, said securement elements and said interposer being formed integrally with one another as a single sheetlike unit.

26. A chip assembly as claimed in claim 24 or 25 further characterized in that at least a portion of

each said securement element is disposed outboard of said chip, the assembly further comprising at least one support element disposed alongside said chip in alignment with said at least one securement element, each said support element having a front surface facing and supporting one of said securement elements.

27. A chip assembly as claimed in claim 27 further characterized by a plurality of outside terminals mounted on said at least one securement element, and outside terminal leads extending between said outside terminals and some of said peripheral contacts on said chip.

28. A chip assembly as claimed in claim 27 further characterized by a compliant layer disposed below said central terminals and a compliant layer disposed below said outside terminals.

29. A semiconductor chip assembly of the type including a semiconductor chip having a front surface and a plurality of contacts disposed in a pattern on said front surface, said pattern encompassing a contact pattern area on said front surface, sheetlike dielectric interposer overlying said front surface of said chip, said interposer having a first surface facing toward said chip and a second surface facing away from said chip characterized by an area of said interposer overlying said contact pattern area of said chip, said interposer having apertures extending from said first surface to said second surface, a plurality of terminals disposed in a pattern on said second surface of said interposer, at least some of said terminals being disposed in said area of said interposer overlying said contact pattern area, each such terminal being associated with one of said contacts on said chip and a flexible conductive lead extending between each said terminal and the associated one of said contacts, each such lead extending through one of said apertures, each said lead having a contact end connected to the associated contact and a terminal end connected to the

associated terminal, said terminals being movable relative to the contact ends of said leads.

30. A chip assembly as claimed in claim 29 further characterized in that each said terminal is disposed adjacent one of said apertures in said interposer, and each said lead extends from one said terminal, through the adjacent aperture to one of said contacts on said chip.

31. A chip assembly as claimed in claim 29 or 30 further characterized in that each said lead is curved in a direction parallel to said front surface of said chip.

32. A chip assembly as claimed in claim 29 or 30 further characterized in that each said lead is curved in a direction perpendicular to said front surface of said chip.

33. A chip assembly as claimed in claim 29 or 30 or 31 or 32 further characterized in that said terminals are substantially evenly distributed throughout an area of said interposer overlying said front surface of said chip.

34. A chip assembly as claimed in claim 33 or 33 further characterized in that a substrate facing toward said interposer and a plurality or connection pads disposed in a pattern corresponding to the pattern of said terminals so that said pads confront said terminals on said interposer and means for bonding said pads on said substrate to said terminals on said interposer.

35. A chip assembly as claimed in claim 34 wherein said means for connecting said terminals to said pads of said substrate includes a mass of electrically conductive bonding material disposed between each said terminal and the associated contact pad of said substrate.

36. A method of making a semiconductor connection component characterized by the steps of:

(a) providing a sheetlike dielectric element having first and second surface and one or more apertures extending between said surfaces;

(b) laminating a conductive sheet to said second surface of said element, so that a first surface of said sheet confronts said second surface of said element and so that said sheet overlies said one or more apertures;

(c) forming a resist pattern on a second surface of said sheet facing away from said element, said resist pattern including lead areas at least partially aligned with said one or more apertures and terminal areas contiguous with said lead areas but not aligned with said one or more apertures;

(d) applying a resist to the first surface of said conductive sheet in said one or more apertures;

(e) contacting said conductive sheet with an etchant so that said etchant removes said conductive sheet except in said lead areas and said terminal areas; and

(f) removing said resists, to thereby leave said lead portions of said conductive sheet as leads projecting into said apertures.

37. A method as claimed in claim 36 further characterized in that said step of applying a resist to the first surface is performed by laminating a sheet of resist to said first surface of said so that the resist of said sheet fills said one or more apertures.

38. A method of making a sheetlike dielectric element with prefabricated electrically conductive leads thereon characterized by the steps of providing a dielectric layer of said element with features which project vertically out of the plane of said sheetlike element, depositing conductive material on said dielectric layer so that said conductive material forms leads extending across said projecting features, and then selectively removing the portions of said dielectric layer constituting said projecting features,

to thereby from said prefabricated leads to bends projecting out of the plane of said sheetlike element.

39. A semiconductor chip assembly of the type including:

(a) a semiconductor chip having oppositely-facing front and rear surfaces, edges extending between said front and rear surfaces and contacts on said front surface, characterized by;

(b) a generally sheetlike backing element underlying said chip, said backing element having a top surface facing toward said chip and a bottom surface facing away from said chip, said backing element having a central region aligned with said chip and terminals, at least some of said terminals being disposed in said central regions; and

(c) electrically conductive leads interconnecting said contacts on said chip front surface and said terminals on said backing element bottom surface, said leads extending alongside said edges, said backing element and leads being flexible so that said terminals on said backing element are movable with respect to said chip.

40. A chip assembly as claimed in claim 39 further characterized by at least one generally sheetlike, flexible flap extending upwardly alongside one edge of said chip, each said lead including a flap portion extending along one said flap.

41. A chip assembly as claimed in claim 40 further characterized in that said contacts on said chip include at least one elongated row extending adjacent one said edge of said chip and each said flap extends to the vicinity of one said row.

42. A chip assembly as claimed in claim 41 further characterized in that each said flap includes an electrically conductive layer and a dielectric layer disposed between said electrically conductive layer and said flap portions of said leads.

43. A chip assembly as claimed in claim 42 further characterized in that said backing element includes an electrically conductive layer and a dielectric layer, each said lead including a backing element portion extending along said backing element between the flap portion of such lead and one of said terminals, said dielectric layer of said backing element being disposed between the conductive layer of the backing element and said backing element portions of said leads.

44. A chip assembly as claimed in claims 40, or 41, or 42 or 43 further characterized by at least one substantially rigid support element, each said support element being disposed alongside one edge of said chip.

45. A chip assembly as claimed in claim 51 further characterized in that said at least one flap includes a plurality of flaps and said at least one support element includes a plurality of support elements, said plural support elements being connected to one another and cooperatively defining a box surrounding said chip.

46. A chip assembly as claimed in claim 45 further characterized by a generally planar floor element extending between said support elements beneath said chip, said floor element being connected to said support elements so that said floor element defines the floor of said box and said support elements constitute the walls of the box, said chip being disposed within said box, said backing element and flaps being disposed on the outside of said box.

47. A chip assembly as claimed in claim 39 further characterized by substrate having a top surface facing said backing element and a plurality of connection pads disposed on said top surface, said terminals on said backing element and said connection pads on said top surface being disposed in corresponding patterns so that one said terminal is aligned with each one of said connection pads, the assembly additionally

comprising means for connecting said connection pads on said substrate to said terminals on said backing element.

48. A chip assembly as claimed in claim 39 further characterized by an interposer overlying the front surface of said chip, said interposer having terminals thereon electrically connected to said chip or to said terminals on said backing element.

49. A circuit assembly comprising a plurality of chip assemblies as claimed in claim 48, said chip assemblies being arranged in a stack having a top and a bottom, whereby said chip assemblies include a bottom one of said chip assemblies at the bottom of said stack and one or more non-bottom chip assemblies, each said non-bottom chip assembly overlying another, immediately subjacent one of said chip assemblies, the backing element of each such non-bottom chip assembly facing the interposer of the immediately subjacent one of said chip assemblies, at least some of the terminals on the backing element of each said non-bottom chip assembly being connected to the terminals on the interposer of the immediately subjacent chip assembly, whereby the chips of said chip assemblies are electrically connected to one another.

50. A component for mounting a semiconductor chip of the type including:

(a) a flexible sheetlike backing element having a plurality of terminals thereon, characterized by;

(b) at least one substantially rigid support element projecting upwardly from said backing element, each said support element having a top edge remote from said backing element; and

(c) a plurality of leads connected to said terminals and extending upwardly alongside at least one of said support elements.

51. A component as claimed in claim 50 further characterized in that said at least one support

element includes a plurality of walls defining a box having a top and a bottom, said backing element being positioned adjacent the bottom of said box, said leads extending upwardly toward the top of the box, said box being open at the top whereby a semiconductor chip may be inserted into the box.

52. A component as claimed in claim 51 further comprising a plurality of generally sheetlike flaps extending upwardly from said backing element alongside said walls, said leads extending along said flaps.

53. A component as claimed in claim 52 further characterized by a floor element extending between said support elements, said backing element being disposed beneath said floor element.

54. A component as claimed in claim 53 further characterized by an electrically conductive layer incorporated in each said flap and in said backing element.

55. A component as claimed in claim 51 or 52 or 53 or 54 further comprising a compliant layer overlying said backing element.

56. A method of making a semiconductor chip assembly of the type including the step of:

(a) positioning a generally sheetlike, flexible backing element so that a top surface of the backing element faces towards a rear surface of the chip and so that terminals in a central region of said backing elements are aligned with said chip, characterized by the step of;

(b) connecting said terminals on said backing element to contacts on a front surface of said chip, facing away from said rear surface and said backing elements, by connecting electrically conductive leads between said contacts and said terminals so that said electrically conductive leads extend alongside edges of said chip.

57. A method as claimed in claim 56 further characterized in that said connecting step includes the step of positioning at least one generally sheetlike flap alongside at least one edge of said semiconductor chip so that flap portions of said leads extending on each said generally flap extend from said backing element towards said front surface of said chip.

58. A method as claimed in claim 57 further characterized in that said step of positioning said flap includes the step of positioning each said flap so that the flap portions of leads disposed thereon extend to the vicinity of a row of contacts on the front surface of said chip and said connecting step further includes the step of wire bonding each said row of contacts to the adjacent flap portions of said leads, said wire bonding step including the steps of detecting the actual positions of said flap portions of said leads relative to said contacts on said chip after said step of positioning said at least one flap and controlling said wire bonding step in accordance with said detected relative positions.

59. A method as claimed in claim 57 further characterized in that said step of positioning said backing element includes the step of positioning the chip within a box incorporating a plurality of walls projecting upwardly from said backing element so that said front surface of said chip faces away from said backing element and said rear surface of said chip faces towards said backing element, said box having a plurality of said flaps extending upwardly from said backing element alongside said walls, whereby said flaps will be positioned alongside the edges of said chip when said chip is positioned in said box.

60. A method as claimed in claim 56 further characterized by the steps of providing a compliant layer between said terminals and said bottom surface of said chip, and electrically testing the assembly by simultaneously engaging a plurality of said terminals

with a plurality of test pins so that said test pins make electrical contact with said terminals, whereby said compliant layer will be compressed in said engaging step.

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